REMARKS

Claims 90, 93-125 and 128-141 are pending in this application. Claims 122 and 137 have been amended. No new matter has been introduced. Applicants acknowledge with appreciation the indication in the October 9, 2007 Office Action that claims 90, 93-121 and 130-136 are allowable.

Claims 122-125, 128, 129 and 137-141 stand rejected under 35 U.S.C. §103 as being unpatentable over Rhodes (U.S. Patent No. 6,204,524) ("Rhodes") in view of Lauxtermann et al. (U.S. Patent Pub. No. 2001/0015831) ("Lauxtermann"). This rejection is respectfully traversed.

The claimed invention relates to a method of forming a CMOS imager with improved charge storage. As such, amended independent claim 122 recites a "method of forming an imager" by *inter alia* "forming a photosensor including a charge collection region . . . adjacent one side of a gate of a pixel transistor" and "forming a floating diffusion region for receiving charge from said charge collection region, said floating diffusion region being connected to said gate of said pixel transistor and being adjacent another side of said gate opposite said charge collection region." Amended independent claim 122 also recites "forming a charge storage capacitor . . . so that one electrode of said storage capacitor is connected directly to said floating diffusion region by an electrical contact and the other electrode of said storage capacitor is connected directly to a gate of another transistor."

Amended independent claim 137 recites a "method of forming an imager" by *inter alia* "forming a photosensor including a charge collection region . . . adjacent one side of a gate of a pixel transistor," "forming a floating diffusion region . . . connected to said

gate of said pixel transistor and being adjacent another side of said gate opposite said charge collection region" and "directly connecting an electrode of a first charge storage capacitor to said floating diffusion region by a first electrical contact." Amended independent claim 137 further recites "directly connecting an electrode of a second charge storage capacitor to said charge collection region by a second electrical contact."

Rhodes relates to a CMOS imager that "provides improved charge storage by fabricating a storage capacitor in parallel with the photocollection area of the imager." (Abstract). According to Rhodes, "[t]he storage capacitor may be a flat plate capacitor formed over the pixel, a stacked capacitor or a trench imager formed in the photosensor." (Abstract).

Lauxtermann relates to "a method for operating a CMOS image sensor including a matrix of pixels (50) arranged in a plurality of lines and columns, each of said pixels including a photosensor element (PD) accumulating charge carriers in proportion to the illumination thereof and storage means (C1,55) able to be coupled to said photosensor element (PD) at a determined instant in order to generate a sampled signal representative of said charge carriers accumulated by the photosensor, the storage means (C1, 55) being intended to assure storage for the purpose of reading said sampling signal." (Abstract). According to Lauxtermann, "when said sampled signal, stored across said storage means is read, the photosensor element is held at a voltage such that any charge carrier generated by the latter is drained and thus does not disturb the sampled signal stored on the storage means." (Abstract).

The subject matter of claims 122-125, 128, 129 and 137-141 would not have been obvious over Rhodes in view of Lauxtermann. In the present case, Rhodes and

Lauxtermann, alone or in combination, do not disclose or suggest the subject matter of independent claims 122 and 137 and of their dependent claims.

Rhodes does not disclose, teach or suggest "forming a photosensor including a charge collection region . . . adjacent one side of a gate of a pixel transistor" and "forming a floating diffusion region for receiving charge from said charge collection region, said floating diffusion region being connected to said gate of said pixel transistor and being adjacent another side of said gate opposite said charge collection region," much less "forming a charge storage capacitor . . . so that one electrode of said storage capacitor is connected directly to said floating diffusion region by an electrical contact and the other electrode of said storage capacitor is connected directly to a gate of another transistor," as claim 122 recites.

Storage capacitor 162 of Rhodes, which would arguably correspond to the "charge storage capacitor" of the claimed invention, is connected to a fifth doped region 155 ("which is formed adjacent to the photogate 102") and not to the floating diffusion region 130. Region 155 of Rhodes is not a "floating diffusion region . . . connected to a gate of a pixel transistor," as in the claimed invention. In addition, no electrode of the storage capacitor 162 of Rhodes is connected directly to a floating diffusion region "by an electrical contact," while the other electrode is directly connected to "a gate of another transistor," as in the claimed invention.

Lauxtermann fails to supplement the deficiencies of Rhodes. Lauxtermann relates to a method of maintaining constant the sampled charge stored in memory node 55 during the read process (¶[0010]), and not to methods of forming CMOS imagers, much less to methods of forming CMOS imagers by the specific steps of the claimed invention.

Lauxtermann is also silent about a capacitor that has one electrode "connected directly to said floating diffusion region by an electrical contact and the other electrode . . . connected directly to a gate of another transistor," as claim 122 recites.

Rhodes and Lauxtermann, considered alone or in combination, also fail to disclose, teach or suggest all limitations of claim 137 and of dependent claims 138-141. None of the cited references teaches or suggests a method of forming an imager by *inter alia* forming first and second capacitors, and connecting the electrodes of each of the two capacitors in a particular manner, as in the claimed invention. Rhodes is silent about a "first charge storage capacitor" and a "second charge storage capacitor," much less about "directly connecting an electrode of a first charge storage capacitor to said floating diffusion region by a first electrical contact" and "directly connecting an electrode of a second charge storage capacitor to said charge collection region by a second electrical contact." Rhodes teaches only one capacitor structure (i.e., capacitor 162) formed overlying an active area of the pixel sensor cell, and not first and second charge storage capacitors, as in the claimed invention.

Lauxtermann also teaches only one capacitor, and not first and second capacitors having their electrodes connected to the floating diffusion region and to the charge collection region, as in the claimed invention.

In the Office Action dated October 9, 2007, the Examiner asserts that Lauxtermann discloses "one electrode (top of drawing) of a charge storage capacitor [C1] . . . connected directly to said floating diffusion region (55) by an electrical contact and the other electrode (bottom in drawing) . . . connected . . . to a gate of a transistor (M4; a capacitive connection is established)." (October 9, 2007 Office Action at 3). Applicants

submit that, as clearly illustrated in Figure 2B of Lauxtermann, one electrode of capacitor C1 is connected to pixel memory node 55, while the other electrode of capacitor C1 is connected to ground. Thus, Lauxtermann fails to disclose or suggest a capacitor connected in the manner of the claimed invention, much less a first and second capacitors connected in the manner of the claimed invention.

In the Office Action dated October 9, 2007, the Examiner also asserts that the "arguments that 'Rhodes teaches only one capacitor' and 'Lauxtermann also teaches only one capacitor' are against the references individually and cannot be the basis of showing nonobviousness since the rejections are based on combinations of references." (October 9, 2007 Office Action at 7). Applicants submit that, even if Rhodes and Lauxtermann are combinable, the combined teachings still do not disclose or suggest a capacitor having two electrodes, one electrode connected to a floating diffusion region and the other electrode connected to a transistor gate. In fact, none of the capacitive structures of Rhodes and Lauxtermann has an electrode connected to a transistor gate, as in the claimed invention. Thus, Applicants do not argue against the references individually; Applicants simply argue that the references (even when combined) do not disclose all limitations of the claimed invention. The combined teachings also do not disclose or suggest two capacitors as part of an imager, the two capacitors having capacitor electrodes connected in the manner claimed in claim 137, for example.

For at least these reasons, the Office Action fails to establish a *prima facie* case of obviousness. Withdrawal of the rejection of claims 122-125, 128, 129 and 137-141 is respectfully requested.

Allowance of all pending claims is solicited.

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Respectfully submitted,

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